(a) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent, load paths being arranged in series and between a first and second supply potential, and a centre tap connected with an output terminal of the integrated circuit; and

B3 cont'd

(b) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

Please add the following new claims:

6. (New) A circuit for generating a negative signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

B4

(a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply

potential for receiving a negative control pulse at the control terminal;

(b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-up resistor connected between the first supply potential and the output terminal for generating a negative signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

7. (New) A circuit according to claim 6 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

8. (New) A circuit according to claim 6 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.

9. (New) A circuit for generating a positive signal pulse in response to receiving a sequence of a positive and negative control pulse, the circuit comprising:

(a) a first transistor including a control terminal and a load path connected between an output terminal and a first supply potential for receiving a negative control pulse at the control terminal;

(b) a second transistor including a control terminal and a load path connected between the output terminal and a second supply potential having a potential less than the first supply potential for receiving a positive control pulse at the control terminal in a sequence with the control terminal of the first transistor receiving the negative control pulse; and

(c) a pull-down resistor connected between the second supply potential and the output terminal for generating a positive signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses.

10. (New) A circuit according to claim 9 wherein a waiting time is provided between the sequence of negative and positive control pulses such that the control pulses do not overlap.

11. (New) A circuit according to claim 9 further including an inverter delay device for generating one of the first and second control pulses from the other of the two control pulses.